CHIP SCALE PACKAGES

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ABSTRACT

A chip scale package structure formed by adhering a glass sheet having a pattern of holes matching a pattern of bond pads on a semiconductor wafer so that the pattern of holes on the glass sheet are over the pattern of bond pads on the semiconductor wafer. Metallized pads are formed on the glass sheet adjacent to each hole and in one embodiment a conductive trace is formed from each metallized pad on the glass sheet to the bond pad on the semiconductor wafer under the adjacent hole. In a second embodiment, a pad is formed on the glass sheet adjacent to each hole and the pad extends down the sides of the adjacent hole. The hole is filled with a metal plug that electrically connects the pad on the glass sheet to the bond pad on the semiconductor wafer. In each embodiment, a solder ball is formed on each pad on the glass sheet.